

## TRANSFORMATION OF A PERIODIC SIGNAL INTO AN ADJUSTABLE-FREQUENCY SIGNAL

### PRIORITY CLAIM

[1] This application claims priority from French patent application  
5 No. 02/11418, filed September 13, 2002, which is incorporated herein by reference.

### BACKGROUND OF THE INVENTION

#### FIELD OF THE INVENTION

[2] The present invention relates generally to devices for transforming a periodic reference signal into a signal of adjustable frequency.

#### DISCUSSION OF THE RELATED ART

[3] Such devices are for example used in circuits of serial data  
10 transmission between a computer and hard disks.

[4] The data to be transmitted come from the computer core in parallel on each transmission circuit generally via a so-called PCI (peripheral communication interface) bus. At the output of each transmission circuit, a serializer transmits serial data onto a connection cable such as a coaxial cable or an fiber optic connection.

15 [5] To limit electromagnetic emission upon transmission of data on the connection cables, the serial data may be transmitted at variable frequency. Conventionally, the transmit frequency varies between a reference frequency, for example, 1 GHz, and a frequency slower by at most 5%, for example, 995 MHz. The frequency modulation is periodic, the modulation frequency currently ranging  
20 between 30 and 33 kHz.

[6] Based on a reference clock signal, which oscillates at the reference frequency, a transformation device provides a clock signal having a serialization frequency controlling the serializer.

25 [7] Some known frequency transformation devices are formed with a phase-locked loop or PLL.

[8] A disadvantage of such devices is that their surface area may be very large.

[9] Further, such devices generally comprise analog circuits: a voltage-controlled oscillator and a low-pass filter. The analog circuits typically must be 5 adapted to each integrated circuit technology, and the operation of such circuits in all possible configurations, especially of temperature, manufacturing process, and supply voltage, poses more problems than that of all-digital circuits.

#### SUMMARY OF THE INVENTION

[10] One embodiment of the present invention provides a frequency-transformation device of low bulk.

[11] Another embodiment of the present invention provides such a device, which is entirely digital.

[12] Another embodiment of the present invention provides such a device of simple structure.

[13] More specifically, an embodiment of the present invention is a device 15 for transforming a periodic input signal into an output signal of distinct frequency, comprising two adjustable delay means receiving the input signal, the difference between the maximum and minimum delays of each delay means being greater than one period of the input signal, a multiplexer selecting the output signal of one or the 20 other of the delay means, control means for, according to whether the frequency of the output signal must be smaller or greater than the frequency of the input signal, increasing or decreasing at the rate of the input signal, or at a multiple of this rate, the delay of the selected delay means, and controlling a minimum or maximum delay for the delay means which has not been selected, and a phase comparator 25 adapted to changing the multiplexer selection when the transitions of the signals output by the delay means corresponding to a same transition of the input signal are offset by a duration greater than or equal to one period of the input signal.

[14] According to an embodiment of such a transformation device, the 30 control means comprise means for setting the increase or decrease rate of the delay of the delay means.

**[15]** According to an embodiment of such a transformation device, the delay of the delay means is capable of varying by increments or decrements and the control means comprise means for setting the increment or decrement value.

**[16]** According to an embodiment of such a transformation device, each 5 delay means comprises several delay elements in series, the output of each delay element being connected to the output of the delay means via a switch, the input of the first delay element being connected to the input of the delay means.

**[17]** According to an embodiment of such a transformation device, the phase comparator comprises two NAND gates with two inputs, the output of a NAND 10 gate being connected to a first input of the other NAND gate, each NAND gate receiving on its second input one of the output signals of said delay means, one of these signals being transmitted to the control input of a first flip-flop via a non-inverting circuit exhibiting a delay, the output of one of the NAND gates being connected to the data input of the first flip-flop, the output of the first flip-flop 15 controlling a second flip-flop having its output connected to its input via an inverter, the output of the second flip-flop controlling the multiplexer of the transformation device.

**[18]** According to an embodiment of such a transformation device, the delay of one of the delay means increases or decreases only during one or several 20 cycles of a set of cycles of the input signal, the number of increases or decreases of the delay over a set of cycles being all the greater as the frequency of the output signal is remote from the frequency of the input signal.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[19]** Features and advantages of the present invention will be discussed in detail in the following non-limiting description of specific embodiments in connection 25 with the accompanying drawings.

**[20]** FIG. FIG. 1 is a diagram of a frequency-transformation device according to an embodiment of the present invention;

[21] FIG. FIG. 2 is a diagram illustrating the shape of the signals at various points of the device of FIG. FIG. 1 according to an embodiment of the present invention;

[22] FIG. FIG. 3 is a diagram of an embodiment of a delay means of the 5 device according to an embodiment of the present invention;

[23] FIG. FIG. 4 is a diagram of an embodiment of the phase comparator of the device according to an embodiment of the present invention; and

[24] FIG. 5 is a diagram illustrating the signals at various points of the device of FIG. 1 according to an alternative use of the device according to an 10 embodiment of the present invention.

#### DETAILED DESCRIPTION

[25] FIG. 1 is a diagram of a device 10 for transforming a reference clock signal CLK<sub>ref</sub> of frequency f<sub>ref</sub> and of period T into a clock signal CLK<sub>s</sub> of frequency f<sub>s</sub> different from f<sub>ref</sub>. Device 10 comprises two adjustable delay means 11 (DEL1) and 12 (DEL2), which receive signal CLK<sub>ref</sub> and respectively provide signals S<sub>1</sub> and S<sub>2</sub>. 15 Signal S<sub>1</sub> is delayed with respect to CLK<sub>ref</sub> by a delay DEL1 adjustable by a control of a control circuit (CONT) 13. Signal S<sub>2</sub> is delayed with respect to CLK<sub>ref</sub> by a delay DEL2 adjustable by a control of a control circuit (CONT) 14. A multiplexer (MUX) 15 receives signal S<sub>1</sub> on its "0" input and signal S<sub>2</sub> on its "1" input. A selection signal Φ<sub>M</sub> controls multiplexer 15 which provides clock signal CLK<sub>s</sub>. A phase comparator (P) 20 16 receives signals S<sub>1</sub> and S<sub>2</sub> and provides selection signal Φ<sub>M</sub>. Control circuits 13 and 14 are identical and receive clock signal CLK<sub>ref</sub>, selection signal Φ<sub>M</sub>, as well as a control signal Φ<sub>C</sub> indicating the desired frequency.

[26] FIG. 2 is a diagram of signals CLK<sub>ref</sub>, S<sub>1</sub>, S<sub>2</sub>, Φ<sub>M</sub> and CLK<sub>s</sub> of the device of FIG. 1, in the case where the searched frequency f<sub>s</sub> is smaller than 25 reference frequency f<sub>ref</sub>. Reference clock signal CLK<sub>ref</sub> is periodic, with in this example a duty cycle of 50%. Six full periods of CLK<sub>ref</sub> are shown in FIG. 2. Initially, at a time t<sub>0</sub>, selection signal Φ<sub>M</sub> is at level "0" and signal S<sub>1</sub> is selected. Delay DEL2 of delay means 12 is minimum and equal to T/4. Delay DEL1 of delay means 11 progressively increases by T/4, at frequency f<sub>ref</sub>. The first shown rising edges of

signals  $S_1$  and  $CLK_{ref}$  are offset by one half reference period ( $2T/4$ ). The 2<sup>nd</sup> rising edges of signals  $S_1$  and  $CLK_{ref}$  are offset by  $3T/4$ . The 3<sup>rd</sup> rising edges of signals  $S_1$  and  $CLK_{ref}$  are offset by  $T$ . The 4<sup>th</sup> rising edges of signals  $S_1$  and  $CLK_{ref}$  are offset by  $5T/4$ .

5 [27] During all this time, signal  $S_2$  is offset by  $T/4$  with respect to signal  $CLK_{ref}$ . Multiplexer **15** provides signal  $S_1$  until the fourth rising edge of  $S_1$  comes up. At this time  $t_1$ , the 4<sup>th</sup> rising edges of signals  $S_1$  and  $S_2$  corresponding to the offset of the fourth rising edge of signal  $CLK_{ref}$  are offset by one reference period  $T$ . Phase comparator **16** then switches selection signal  $\Phi_M$  from 0 to 1 and the multiplexer 10 selects signal  $S_2$ . At the next rising edge of signal  $CLK_{ref}$ , that is, at the sixth rising edge shown at a time  $t_2$ , delay DEL2 of delay means **12** is increased and the 6<sup>th</sup> rising edges of signals  $S_2$  and  $CLK_{ref}$  are offset by one half reference period ( $2T/4$ ) while delay DEL1 remains constant and equal to  $T/4$ .

15 [28] Delay DEL2 increases until the rising edges of signals  $S_1$  and  $S_2$  corresponding to a same rising edge of  $CLK_{ref}$  are offset by period  $T$ . At this time, the selection switches back.

20 [29] The period of clock signal  $CLK_s$  is thus equal in this example to one reference period plus one quarter, that is,  $5T/4$ . Frequency  $f_s$  thus is equal to 800 MHz when the reference frequency is 1 GHz.

25 [30] Phase comparator **16** of transformation device **10** of FIG. 1 thus has the function of detecting the time at which the rising edges of signals  $S_1$  and  $S_2$  corresponding to a same rising edge of clock signal  $CLK_{ref}$  are offset by a duration greater than or equal to one reference period  $T$ . Phase comparator **16** then changes the level of selection signal  $\Phi_M$ . The previously-selected delay means takes a minimum delay ( $T/4$ ). The delay of the newly selected delay means increases.

[31] Generally, phase comparator **16** can detect the time at which determined transitions, a rising or falling edge, of signals  $S_1$  and  $S_2$  corresponding to a same transition of signal  $CLK_{ref}$ , are offset by at least one period  $T$ .

30 [32] Control circuits **13** and **14** may be formed by means of a finite state machine adapted to increasing the delay of the selected delay means at the rate of signal  $CLK_{ref}$  and positioning the other delay means on the minimum delay.

[33] FIG. 3 is a diagram of an embodiment of delay means 11, 12 used in transformation device 10 according to the present invention. The delay means comprises n delay elements D<sub>1</sub> to D<sub>n</sub> in series, input E of the delay means being connected to the input of delay element D<sub>1</sub>. A delay element may for example be formed of two inverters in series. The output of a delay element D<sub>i</sub>, i ranging between 1 and n, is connected to output S of the delay means via a switch a<sub>i</sub>. The minimum delay between E and S is obtained by turning on switch a<sub>1</sub> and by turning off all the other switches. The delay between E and S can be progressively increased by successively selecting switches a<sub>2</sub>, a<sub>3</sub>, and so on.

10 [34] The number of delay elements is such that the difference between the maximum delay obtained by selecting switch a<sub>n</sub> and the minimum delay obtained by selecting switch a<sub>1</sub> is greater than one reference period T to ensure a proper operation of device 10. The selected delay means changes at the latest when the delay of the selected delay means is maximum.

15 [35] There also exist more sophisticated delay means, such as that described in French patent application 9711022 of the applicant. This French patent is incorporated by reference.

[36] FIG. 4 is a diagram of an embodiment of phase comparator 16 of the transformation device of the present invention. Phase comparator 16 comprises two NAND gates 20 and 21 with two inputs. The output of NAND gate 20 is connected to an input of NAND gate 21 and the output of NAND gate 21 is connected to an input of NAND gate 20. The second input of NAND gate 20 receives signal S<sub>1</sub> and the second input of NAND gate 21 receives signal S<sub>2</sub>. Signal S<sub>1</sub> is transmitted to the control input of a flip-flop 22 via a non-inverting circuit 23 exhibiting a given delay.

20 The output of NAND gate 20 is connected to data input D<sub>1</sub> of flip-flop 22. Output Q<sub>1</sub> of flip-flop 22 controls a flip-flop 24 assembled as a counter, output Q<sub>2</sub> of flip-flop 24 being connected to its data input D<sub>2</sub> via an inverter 25. Output Q<sub>2</sub> of flip-flop 24 provides selection signal  $\Phi_M$  which controls multiplexer 15 of frequency transformation device 10.

25 The output of NAND gate 20 is connected to data input D<sub>1</sub> of flip-flop 22. Output Q<sub>1</sub> of flip-flop 22 controls a flip-flop 24 assembled as a counter, output Q<sub>2</sub> of flip-flop 24 being connected to its data input D<sub>2</sub> via an inverter 25. Output Q<sub>2</sub> of flip-flop 24 provides selection signal  $\Phi_M$  which controls multiplexer 15 of frequency transformation device 10.

30 [37] Outputs Q<sub>1</sub> and Q<sub>2</sub> of flip-flops 22 and 24 are initially positioned at "1" and "0" via for example initialization signals (set, reset). As long as signals S<sub>1</sub> and S<sub>2</sub>

are offset by less than one half-period ( $T/2$ ), output  $Q_1$  of flip-flop **22** remains at 1. At the time when the offset of signals  $S_1$  and  $S_2$  exceeds one half period, output  $Q_1$  of flip-flop **20** switches from 1 to 0. As long as the offset of signals  $S_1$  and  $S_2$  remains between one half-period ( $T/2$ ) and one period  $T$ , output  $Q_1$  of flip-flop **20** remains at 0. Then, when signals  $S_1$  and  $S_2$  are offset by at least one period  $T$ , output  $Q_1$  of flip-flop **22** switches from 0 to 1. Output  $Q_2$  of flip-flop **24** switches state. Since selection signal  $\Phi_M$  switches state, the selection of multiplexer **15** inverts. Signals  $S_1$  and  $S_2$  are progressively offset again and output  $Q_1$  of flip-flop **22** switches back from 1 to 0 and from 0 to 1 and the multiplexer selection inverts again.

10 [38] **FIG. 5** illustrates, as an example, another possible diagram of the signals of the transformation device **10** according to another embodiment of the present invention. In the case where a variable frequency  $f_s$  relatively close to  $f_{ref}$  is desired to be obtained, it becomes impractical to form a delay means such as shown in **FIG. 3** with delay elements having a very small propagation time, for example, on the order of  $1/f_s$ . Recent technologies of integrated-circuit manufacturing indeed enable forming delay elements having a propagation time at least equal to 10 ps. This embodiment of the present invention then provides a means for providing a clock signal  $CLK_s$  having over  $X$  clock cycles an average frequency equal to the desired frequency  $f_s$ .

20 [39] The diagram of **FIG. 5** is obtained with delay means each formed of six delay elements having an identical propagation time  $\tau$  taken to be equal in the example to  $1/6$  of reference period  $T$  of signal  $CLK_{ref}$ . The 1<sup>st</sup> shown rising edges of signals  $S_1$  and  $CLK_{ref}$  are offset by  $\tau$ . Delay **DEL1** is then increased and becomes  $2\tau$ . The 2<sup>nd</sup> rising edges of signals  $S_1$  and  $CLK_{ref}$  are thus offset by  $2\tau$ . Delay **DEL1** is 25 then unchanged for three cycles of signal  $CLK_{ref}$ .  $\Phi_M$  being initially zero, multiplexer **15** provides signal  $S_1$ . Clock signal  $CLK_s$  has over its first four shown cycles, an average period equal to  $5T/4$ , which corresponds to an average frequency  $f_{s1}$  of  $(4/5)*f_{ref}$ .

30 [40] The 6<sup>th</sup> rising edges of signals  $S_1$  and  $CLK_{ref}$  are offset by  $3\tau$ . Delay **DEL1** of delay means **11** is then constant for the next three cycles of signal  $CLK_{ref}$ .

The average frequency of clock signal  $CLK_s$  between its 5<sup>th</sup> and 9<sup>th</sup> rising edges is identical to the frequency between its 1<sup>st</sup> and 4<sup>th</sup> rising edges and is equal to  $f_{s1}$ .

[41] The 10<sup>th</sup> and 11<sup>th</sup> rising edges of signals  $S_1$  and  $CLK_{ref}$  are offset by  $4\tau$ .

Then, a new increase in delay DEL1 is performed on the 12<sup>th</sup> cycle of signal  $CLK_{ref}$ ,

5 and the 12<sup>th</sup> and 13<sup>th</sup> rising edges of signals  $S_1$  and  $CLK_{ref}$  are offset by  $5\tau$ . Within four cycles of signal  $CLK_s$ , two increments equal to  $\tau$  have been performed, its average frequency  $f_{s2}$  is then smaller and equal to  $(2/3)*f_{ref}$ .

[42] Similarly, an increment of delay DEL1 is performed for the 14<sup>th</sup> and 16<sup>th</sup> cycles of  $CLK_{ref}$ . The 14<sup>th</sup> and 15<sup>th</sup> rising edges of signals  $S_1$  and  $CLK_{ref}$  are

10 offset by  $6\tau$  and their 16<sup>th</sup> and 17<sup>th</sup> rising edges are offset by  $7\tau$ . The average frequency of signal  $CLK_s$  between its 13<sup>th</sup> and 17<sup>th</sup> rising edges is then equal to  $f_{s2}$ .

[43] During all this period, between the 1<sup>st</sup> and the 16<sup>th</sup> rising edge of signal  $CLK_s$ , signal  $S_2$  follows signal  $CLK_{ref}$  with a minimum delay DEL2 equal to  $\tau$ . Output  $Q_1$  of flip-flop 22 of phase comparator 16 is initially at 1. Then, when signals  $S_1$  and

15  $S_2$  are in phase opposition, that is, on the 10<sup>th</sup> rising edge of signal  $S_1$ , output  $Q_1$  switches to zero. At the time when signals  $S_1$  and  $S_2$  are back in phase, that is, on the 16<sup>th</sup> rising edge of signal  $S_1$  and the 17<sup>th</sup> rising edge of signal  $S_2$ , output  $Q_1$  switches to one, and selection signal  $\Phi_M$  initially at "0" switches to "1". Multiplexer 15 provides signal  $S_2$ . Delay DEL1 is then made minimum and equal to  $\tau$ , and delay

20 DEL2 will increase. The 19<sup>th</sup> and 20<sup>th</sup> rising edges of signals  $S_2$  and  $CLK_{ref}$  are offset by  $2\tau$  and their 21<sup>st</sup> and 22<sup>nd</sup> rising edges are offset by  $3\tau$ . Frequency  $f_s$  of signal  $CLK_s$  between its 17<sup>th</sup> and 21<sup>st</sup> rising edges is thus equal to  $f_{s2}$ .

[44] Of course, the above-described embodiments of the present invention are likely to have various alterations, modifications, and improvement which will

25 readily occur to those skilled in the art. In particular, a transformation device according to an embodiment of the present invention may be used to provide a clock signal  $CLK_s$  having a frequency  $f_s$  higher than frequency  $f_{ref}$  of reference clock signal  $CLK_{ref}$ . For this purpose, delays DEL1 and DEL2 of delay means 11 and 12 will be initially maximum. Then the delay of the selected delay means will be progressively

30 decreased, the delay of the other delay means remaining maximum. When the two signals  $S_1$  and  $S_2$  will be back in phase, the selection reverses.

**[45]** Further, those skilled in the art will know how to form other delay means and other phase comparators. For example, one may design the delay means DEL2 so that it does not initially delay the signal S2 relative to CLK<sub>ref</sub>.

**[46]** Moreover, a transformation device — such as the device **10** of **FIG. 1** 5 — according to an embodiment of the invention may be incorporated in an integrated circuit such as a serial-data transmitter or receiver. And such an IC may be incorporated into an electronic system such as a computer system or a data-transmission system.

**[47]** Such alterations, modifications, and improvements are intended to be 10 part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.